PTO/SB/33 (07-05)

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
15114H-071400US

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on December 11, 2009

Signature / J. Matthew Zigmant /

Typed or printed name J. Matthew Zigmant

Application Number	Filed
10/749,910	**December 30, 2003**

First Named Inventor
DHANOA, Kulwinder

Art Unit	Examiner
2181	**LEE, Chun Kuan**

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 44,005.

☐ attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34. _____

/ J. Matthew Zigmant /
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December 11, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☒ *Total of one (1) form is submitted.

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TOWNSEND and TOWNSEND and CREW LLP

By: / J. Matthew Zigmant /

J. Matthew Zigmant

STATEMENT OF REASONS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

PATENT
Attorney Docket No.: 15114H-071400US
Client Ref. No.: A00985

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

DHANOA, Kulwinder

Application No.: 10/749,910

Filed: December 30, 2003

For: SDRAM CONTROLLER

Customer No.: 26059

Confirmation No. 1395

Examiner: LEE, Chun Kuan

Technology Center/Art Unit: 2181

STATEMENT OF REASONS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

This statement is submitted in support of a Pre-Appeal Brief Request for Review, which is submitted here along with a Notice of Appeal. The applicant respectfully requests review of the Final Office Action mailed August 11, 2009 and the Advisory Action mailed December 4, 2009, regarding the rejection of claims 1-2, 5-8, 11-13, and 18-21.

I. Rejection of Claim 1

Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gray in view of Abramson, Iizuka, and Nguyen. But this combination of cited references does not show or suggest "a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request," in combination with the other recited limitations.

The pending office action cites several passages in Iizuka as showing or suggesting this feature, but appears to recognize that Iizuka does not show or suggest that the buffers are sized to store a data burst since Iizuka's buffers are sized to store a number of samples. (See pending office action, page 8, second full paragraph.) The pending office action further cites Gray as showing storing a data burst from memory. (See pending office action, page 2, last paragraph.) The rejection is thus understood to be that since Gray stores data bursts and Iizuka shows buffers sized to hold a number of samples, the combination results in buffers sized to hold data bursts.

The pending advisory action states that the motivation for combining Iizuka and Gray in this manner is "for the benefit of implementing a simplified structure and providing an optimal priority order for data transferring." (See pending advisory action, page 2, third paragraph.)

Iizuka shows that a simplified structure is desired in column 2, lines 26-29. In this passage, Iizuka shows that the simplified structure can be used to "freely edit recorded data without actually rewriting the data." (*id.*) Iizuka further shows that editing data requires cross-fade in order to prevent an unnatural sound. (See Iizuka, column 1, lines 52-59.) These cross-fades have a length of several seconds, and conventionally require data to be rewritten. (id.) Iizuka shows that this rewriting can be avoided by storing data in a cross-fade memory, and reading the data out when required. (See Iizuka, Figure 12 and column 23, lines 28-54.) Accordingly, the simplified structure shown by Iizuka relates to using a cross-fade memory; it does not relate to the sizing of buffers.

Iizuka shows that a priority order for data transferring can be determined in a number of ways, including "a degree of emergency." (See Iizuka, column 32, lines 14-19.)

Iizuka does not show that the priority order is optimized by sizing buffers in any particular manner. Accordingly, there is no motivation to combine the references in the manner suggested to show or suggest that each of the plurality of buffers is sized to store a data burst for a memory access request.

The pending office action recognizes that Abramson does not show or suggest this feature. (See pending office action, page 10, second paragraph.) Nguyen adds nothing to this. Accordingly, the combination of cited references does not show or suggest a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request, as is required by the claim.

Claim 1 further recites "wherein, for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic." The combination of cited references does not show or suggest this feature.

The pending office action cites Figure 8 of Iizuka as showing or suggesting this feature. (See pending office action, page 8, last paragraph.)

In Figure 8, Iizuka shows three buffers, 9-1 to 9-3. (See Iizuka, Figure 8.) Each buffer stores a sample. (See Iizuka, column 11, lines 20-25.) Each buffer is a FIFO operating as a ring buffer. (*id.*) In this configuration, a start and end address for each sample are stored in a buffer 9-1 to 9-3. Data in buffers 9-1 to 9-3 are transferred to a hard drive using DMA transfers. (See Iizuka, Figure 8.)

Thus, Iizuka does not show a wrapping memory access request. Instead, Iizuka shows that each sample is stored in a single buffer. Iizuka does not show that a sample needs to be wrapped using multiple buffers. Because of this, Iizuka does not show that data required for a beginning and end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer. Instead, Iizuka shows that the beginning and end of each sample is stored in its own buffer 9-1 to 9-3.

The advisory office action appears to recognize that Iizuka does not show this feature, and instead appears to indicate that Iizuka in combination with one or more other references shows this feature. (See pending advisory action, page 2, fifth paragraph.) The

motivation for this combination is again "for the benefit of implementing a simplified structure and providing an optimal priority order for data transferring." (*id.*)

Again, Iizuka shows that a simplified structure is provided to avoid rewriting data during a cross-fade and that the priority order can be determined according to a degree of emergency or other criteria. Neither of these concerns suggests that data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer.

Accordingly, the combination of cited references does not show or suggest wherein, for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic, as is required by the claim.

Claim 1 further recites "wherein the control logic records a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer." The combination of cited references does not show or suggest this feature.

The pending office action cites Nguyen as showing or suggesting this feature. (See pending office action, page 9, last paragraph.)

Nguyen shows the use of input and output pointers. (See Nguyen, Figure 2.) The input pointer points to the next slot involved in an input operation, while the output pointer points to the next slot involved in an output operation. (See Nguyen, column 6, lines 4-7.) Nguyen does not show that these pointers allow control logic to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer. Instead, Nguyen shows an input pointer that points to a next slot involved in an input operation and an output pointer that points to the next slot involved in an output operation.

The pending office action appears to recognize that Nguyen does not show this feature, and instead states that the previous office action "relied mainly on Iizuka for the teaching" of this feature. (See pending office action, page 4, second paragraph.) The pending office action further cites several passages in Iizuka. However, as described above, Iizuka does

not show memory wrapping, and thus cannot show a pointer that allows control logic to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer. Moreover, no motivation for combining Iizuka and Nguyen in a manner to show this feature is given in either the pending final office action or the pending advisory action.

The pending office action recognizes that Gray and Abramson do not show or suggest this feature. (See pending office action, page 12, first full paragraph.) Accordingly, the combination of cited references does not show or suggest wherein the control logic records a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer, as is required by the claim.

For at least these reasons, claim 1 should be allowed.

II. Rejection of the Remaining Claims

Claims 7, 13, and 18 should be allowed for similar reasons as claim 1. The remaining rejected claims depend on one of the above claims and should be allowed for at least the same reasons and the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is respectfully requested.

Respectfully submitted,

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